Optimization and Performance Analysis Of Transceiver Front End Low Power Low Noise Amplifier

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ABSTRACT:
A Frequency range of 2.4-2.5 GHz is intentionally reserved for industrial, scientific and medical (ISM) radio purposes. The receiver sensitivity is a function of signal-to-noise ratio, receiver bandwidth and receiver noise figure. Low-noise amplifier (LNA) being the first building block of a front-end receiver after antenna establishes the overall noise figure (NF). The design of the front-end low noise amplifier (LNA) is one of the challenges in Radio Frequency (RF) receivers. Major difficulties of RF CMOS circuit implementation are relatively lower unity-gain frequency and poor noise performances. Many high gain amplifier topologies have been proposed as a way to satisfy the requirement for low power dissipation as well as improved performances. This thesis work focus on Design of Optimized Transceiver Front-end Low Power Low Noise Amplifier in 0.18µm CMOS technology.

Keyword- Low Noise Amplifier (LNA), Mosfet (MOS), Noise figure(NF),

I. INTRODUCTION

Global wireless communication is one of main developments in industry of 21st century. With the progressing and improving of wireless communication technology in recent years, thousands of the diverse classification products make our life more convenient and improve the communication quality. The demand that the mankind combined with information for the communication has been increasing all the time, with the progress of the new technology, appearance of the new specification, the applications of the mobile communication are wider and wider. The WLAN market has been one of the shining stars in the high technology marketplace over the past few years, with enterprises and home-based consumers. The great expansion of mobile computers including Notebook computers and personal digital assistants (PDA's) provide a potential market for mobile LAN connectivity. The use of Wireless LANs in a static environment too has some advantages over cabled networks, such as flexibility and minimal cable installations. Today WLANs are widely recognized as a general-purpose connectivity alternative for a broad range of business customers. Within the wireless hierarchy, short-range wireless technology plays a key role achieving “everybody and everything is connected”. An ever increasing demand of short-range wireless devices with video transfer capability and location-aware applications within home and office environments is observed.

II. LOW NOISE AMPLIFIER

The Low Noise Amplifier (LNA) is a special type of electronic amplifier or amplifier used in communication systems to amplify very weak signals captured by an antenna. It is often located very close to the antenna Radio Frequency front-end receiver block diagram), so that losses in the feed line become less critical. This "active antenna" arrangement is frequently used in microwave systems like GPS; because coaxial cable feed line is very lossy at microwave frequencies.[22]

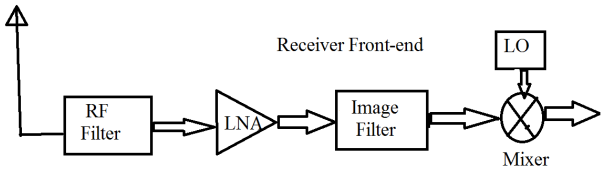

Figure: 2**.1** Radio Frequency front-end receiver block diagram[20]

2.1 LNA Topologies

LNA's performance is more dependent on process technology than on circuit topology. Indeed, LNA usually only involves one or two transistors in its signal path, and there is not much degree of freedom to form deferent architectures. Still, for a fixed technology, deferent circuit structures will produce a deferent performance and design trade-off. Because an LNA's input will directly interface with a RF filter which generally requires certain impedance termination, so input impedance matching is a must requirement for all the LNA's listed. The LNA structures are distinguished from

each other by how the input impedance matching is achieved [21].

2.1.1 Resistive termination:

This achieves input matching by directly placing a 50Ω resistor in parallel with the gate of transistor M1. This is the most straightforward method but the noise figure is exceptionally high.

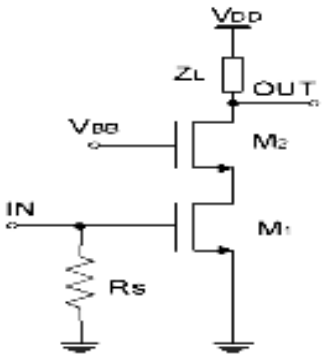

Figure:2.1.1 Resistive termination [15].

So the noise figure is readily larger than 6dB. The primary contribution of noise comes from the termination resistor and transistor drain noise.

2.1.2 Common Base:

This topology is used to realize a wideband LNA. The input impedance is equal to 1/gm, where gm is the transconductance of the MOS transistor, which is the advantage of this topology. The input impedance are just 1/ gm. By carefully choosing the size of the transistor and biasing condition, 50Ω impedance matches is readily obtained. But there is disadvantage of Common gate configuration is high noise figure which means high power consumption also. The induced gate noise will make the noise factor larger, but the drain noise is still the dominant factor.[15]

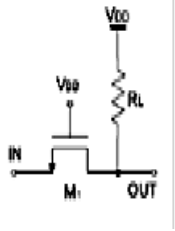

Figure: 1.4.2 Common base [15]

2.1.3 Shunt-Series Feedback:

It utilizes negative shunt feedback to modify the input impedance of a common source stage.

The voltage gain from input to output and is approximately in the order of RL/R1, assuming M1's gm is large enough. The noise figure of this structure is better, but it is still too high to use in some applications. For lower power consumption, drain noise is the major noise contribution, but for high power consumption, gate noise and the noise due to RF also become significant.

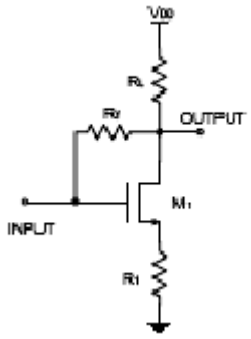

Figure:2.1.3 Shunt-series feedback [15]

2.1.4 Inductive Source-Degeneration:

Wide-band LNA topology exhibit a high NF which result in high power consumption. To achieve lower NF we use narrow-band LNA that is based on the inductively degenerated common source gate.

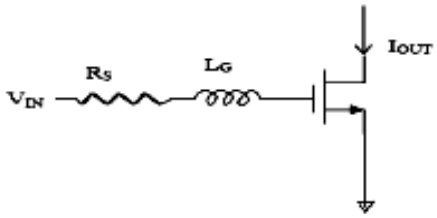

Figure:2.1.4 Gate inductor [21]

It is a very popular narrow-band LNA. It is narrow-band because impedance matching is only established within a very narrow frequency range due to the resonant nature of the reactive matching network. Impedance matching is established by inductive degeneration around operating frequency. The noise figure of this inductive degenerated LNA can be readily made below 2 dB or even lower.In this topology noise is mainly due to the contribution of the drain noise, gate noise and noise due to the correlation between the gate and drain noise.When considering the series resistance of the inductors used in the LNA, an additional term should be added. The noise from series resistance of the degeneration inductor is negligible. Among all the noise contributors, gate noise is the largest one. This is because the gate noise current sees high impedance due to the resonance of the input matching network.

Therefore, in order to reduce the noise factor, value of the input matching network should be limited.

2.2 Wideband vs Narrowband LNA

Because of these two types of matching, we can consider two types of LNA. One uses a narrowband amplifier, and the other uses a wide band amplifier. The matching networks in these two types of LNA differ in their frequency response, one having a wideband response and the other having a narrowband response. Narrowband amplifiers have a tuned matching network at input and output. If integrated with the following stage on chip, sometimes an explicit output matching network can be omitted. Wideband amplifiers, on the other hand, need a wideband matching network. The matching network should compensate for the frequency response of the amplifier so that we can get a flat frequency response at the output. For multistage wideband amplifiers, an inter stage matching network is needed.

The wideband solution consists of designing a general wideband amplifier first. We can then place a band pass filter at its output to achieve band selection. The advantage of this method is that the design work is divided into two independent steps, making each task more manageable and with fewer variables and constraints. A band pass filter with accurate center frequency is easier to achieve because of the wideband characteristics of the amplifier part. The problem with this method is that it unnecessarily demands that the amplifier possess a wideband response, thus making the circuit structure complicated and power hungry. Moreover, the circuit performance, especially the noise performance is poor. On the other hand, for the narrowband approach, after proper narrowband impedance matching and low-noise optimization at the input, not only can we get low-noise performance, but we can also knock down the DC power by a substantial amount. At the output, we use an LC tank circuit to peak the gain so that we can omit the additional gain stage and make the circuit simple. The disadvantage of the narrowband method lies in the difficulty of achieving band pass amplification with accurate center frequency due to circuit element value variation inherent in a very large-scale integration (VLSI) process. This can be resolved by tuning the tank circuit on the chip, Also, there is a need for a low-loss inductor, which has just become available in the modern VLSI process [21].

2.2.1 Narrowband LNA:

Since the signal occupies a narrow bandwidth, we only need to provide impedance matching as well as amplification in this narrow bandwidth. This can be done rather effectively with the process of resonance. Here the reactive part of the impedance is controlled to be nulled out at the resonance frequency, leaving only the resistive part to the resistive source resistance. Since the amplification factor is a product of the device transconductance and load impedance, when the load impedance is controlled to peak up via the resonance process the amplification factor peaks up as a result. There are various ways of achieving resonance. One simple way is the use of an LC tank circuit. This approach has the added advantage in a practical LNA as there already exists in the circuit some parasitic capacitance. The idea, of course, is to add some extra inductance and combine it with this parasitic capacitance, hence achieving resonance. This is especially attractive at RF, since inductance in integrated form and with high Q become say available. This approach basically makes good use of this undesirable parasitic capacitance inherent in the circuit by tuning it out. This is just another way of saying that one makes the resulting capacitance/inductance network possess a zero or infinite impedance at the resonance frequency (a consequence of resonance) and as a result the parasitic capacitance is rendered harmless. In this section, we explain the behavior of the impedance of this network under resonance [21].

2.2.2 Design Parameters of LNA:

Voltage gain: Gain is a measure of the ability of a circuit to increase the power or amplitude of a signal. It is the ratio of output signal to the input signal. It is denoted in terms of decibel(dB).

Voltage Gain= signal output/signal input

$$V_{dB} = 20 \log (V_{out}/V_{in}) \quad (1)$$

Phase margin(PM): The phase margin of an LNA amplifier circuit is the amount of additional phase shift at the closed loop bandwidth required to make the circuit unstable (i.e., phase shift + phase margin = -180°). As phase margin approaches zero, the loop phase shift approaches -180° and the op amp circuit approaches instability.

Power Consumption ($P_{Consumption}$): The total DC power supplied to the LNA amplifier minus the power delivered by the LNA amplifier to its load. To reduce the power dissipation of a CMOS circuit,

the various sources must be identified. There are two types of power consumption relevant to circuit design: the average power and peak power. The peak power is related to the maximum instantaneous current drawn from the supply which can result in large voltage drops/bounces on the resistive power/ground rails. This can badly affect circuit reliability and causes overheating of the devices which degrade the circuit performance. It is therefore essential to have peak power under control. The average power dissipation in a circuit decides the battery size and weight needed to operate the circuit for a given amount of time. Minimizing the average power is more critical than the peak power for almost all low power applications.

Noise performance: There are two main noise performance parameter as given below:

(a)**SNR:** It is the ratio of signal power to the noise power.

SNR= signal power/noise power

(b)**Noise figure:** It is the ratio of SNR at the input to the SNR at the output.

$NF=SNR_{in}/SNR_{out}$

$NF_{(dB)}= 10 \log (SNR_{in}/SNR_{out})$

2.3 Applications of LNA: There are many applications of LNA in wireless communication.

- ISM Radio
- Cellular PCS Handsets
- GPS Receivers
- Cordless Phones
- Wireless LAN
- Wireless Data

III. PROPOSED WORK

For small gain, LNA cannot amplify the incoming weak signal to a desired value, and for large gain, it can degrade the linearity. Some of the design parameters that are commonly considered in LNAs are well. Power consumption is the main function of an LNA in order to overcome the noise of subsequent stages while adding as little inherent noise as possible. Typically, having high gain and low noise in LNAs involves high power dissipation, which is not desirable in portable electronic systems. As a result, in the design process of these circuits there must be trade-off among gain, NF and power consumption. In this thesis I have chosen two architectures, and try to increase the voltage gain and decrease the noise figure by changing inductor values.

3.1 A Low-Power and High-Gain Fully Integrated CMOS LNA

In this thesis, I present the design of a fully integrated CMOS Low Noise Amplifier (LNA) with on-chip spiral inductors in 0.18um CMOS technology for 2.4GHz frequency range. Using cascode configuration, lower power consumption with higher voltage and power gain are achieved. In this configuration, we managed to have a good trade off among low noise, high gain, and stability. Using common gate (CG) configuration, I reduced the parasitic effects of Cgd and therefore alleviated the stability and linearity of the amplifier. This configuration provides more reverse isolation that is also important in LNA design. The LNA presented here offers a good noise performance. Complete simulation analysis of the circuit results in center frequency of 2.4 GHz, with 26.62dB voltage gain, 1.16dB noise figure (NF), 50Ω input impedance, while dissipating 2.65mW at 1.8V power supply.

3.1.1 LNA Design Considerations:

Some of the design parameters that are commonly considered in LNAs are well. Providing sufficient voltage gain with acceptable linearity and power consumption is the main function of an LNA in order to overcome the noise of subsequent stages while adding as little inherent noise as possible. For small gain, LNA cannot amplify the incoming weak signal to a desired value, and for large gain, it can degrade the linearity. Typically, having high gain and low noise in LNAs involves high power dissipation, which is not desirable in portable electronic systems. As a result, in the design process of these circuits there must be trade-off among gain, NF, linearity, and power consumption.

3.1.2 Input Impedance Matching:

In practical cases, the input signal to the LNA usually comes from antennas that are connected to LNA circuit by an unknown length of transmission line. This then requires an amplifier with a reasonably stable input impedance of approximately 50Ω. There are several methods to adjust the input impedance of the amplifiers. Four distinct methods are shown in Fig.4.1 the first technique is adding a resistor at the input terminal of the LNA (Fig4.1a) to provide a 50Ω input resistance. Unfortunately in this technique, the resistor itself produces thermal noise that increases

the amplifier's NF. (Fig.4.1b) shows a common-gate (CG) configuration where the input impedance is determined by the g_m of the transistor. There is drawback for CG topology as well due to high input-referred noise in this configuration. The third technique is using a resistive shunt-series feedback (Fig.4.1c) to set the input and output impedances. Amplifiers incorporating this method generally have high power dissipation compared to others with similar noise performance and require accurate on-chip resistors that actually are not available in CMOS Technology. The final method is inductive degeneration common-source LNA that is depicted in (Fig.4.1d)and we are going to use in our design. This technique does not degrade the amplifier's noise performance and it easily matches the input impedance. Another advantage of this method is its filtering capability on input signal.[15]

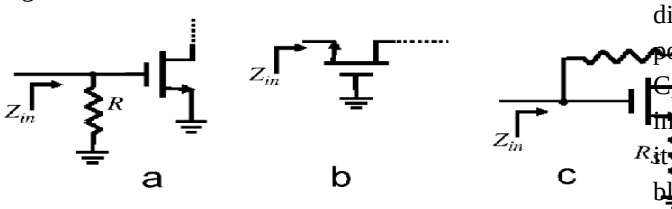

Figure: 3.1 Common LNA architecture. (a) Resistive termination, (b) 1/gm termination, (c) shunt-series feedback, and (d) inductive degeneration [15]

3.1.2 Isolation and Frequency Enhancement:-

In designing RF CMOS amplifiers, the effect of gate– drain overlap capacitance (Cgd) cannot be ignored as it is comparable with the gate–source capacitance (Cgs) in submicron CMOS technologies. It is greatly responsible for the reduction of gain, isolation and the operating frequency of the device. There are various circuit techniques which are used to reduce the effect of this parasitic capacitance by either reducing the flow of reverse signal from it or canceling out what is already passed through it.

Unilateralization method can be achieved using cascade or source-coupled topologies that are depicted in Fig.4.2. These circuits increase bandwidth, reverse isolation and stability but occupy the voltage headroom, reduce voltage swing, and introduce additional noise.[19]

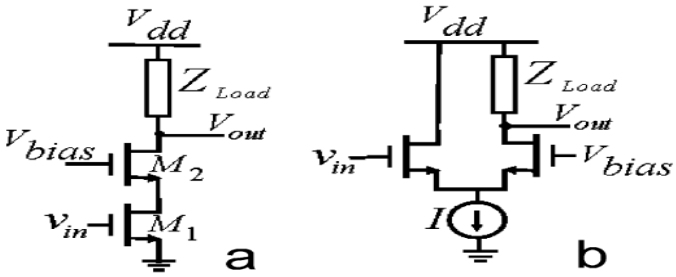

Figure: 4.2 Unilateralization circuits techniques. (a) Telescopic cascade (b) Source coupled [19].

Neutralization technique can be implemented using differential, tuned inductor and transformer-feedback topologies that are depicted in Fig.4.3 All of these methods increase forward gain and reverse isolation for a given power consumption, but do not necessarily reduce the effect of Cgs on the input. In differential neutralization technique C_N makes a positive feedback that can cause instability for $C_N > C_{gs}$. The inductor-tuned technique is usually impractical for monolithic implementation because it requires a relatively large capacitance dc-blocking capacitor. The transformer-feedback technique is not practical because there is not reasonable amount of mutual coupling among integrated inductors.[19]

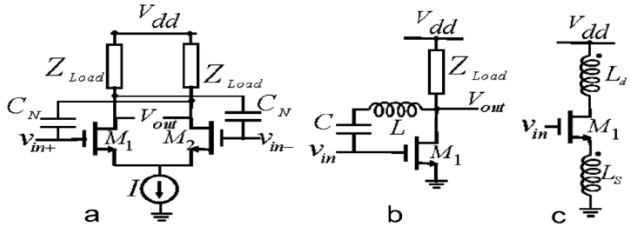

Figure: 4.3 Neutralization circuits techniques. (a) Differential neutralization technique. (b) Tuned inductor technique. (c) Transformer-feedback Technique [19].

Cascode configuration is one of the most widely used techniques to reduce the effect of this capacitance in CMOS RF LNAs. Cascode amplifier is a two stage circuit consisting of a transconductance amplifier followed by a buffer amplifier. The word "cascode" was originated from the phrase "cascade to cathode". This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher

slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect.

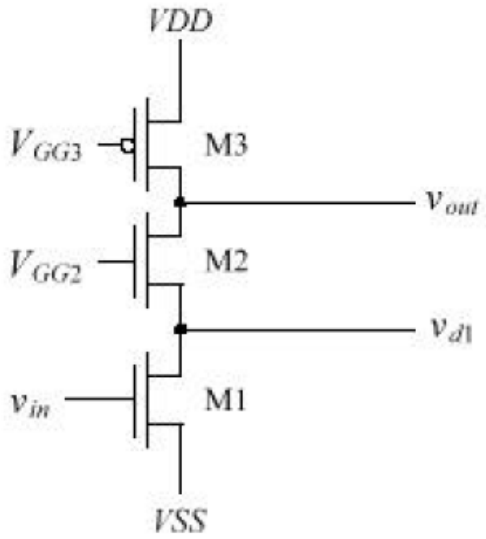

Figure: 3.4 cascode circuits techniques[21]

3.1.3 Design methodology steps of Integrated CMOS LNA:-

With respect to impedance matching and increasing isolation, a good configuration for LNA is the cascode topology with inductive degeneration as depicted in Fig.3.4 There are design steps for fully integrated amplifier as given below:

1. The first design step is calculation of the optimum width of the input transistor to obtain the best noise performance. The channel width of the input transistor is calculated by the following equation:

$$W1= \quad 1/ \quad 3\omega LC_{ox}R_s \quad (2)$$

Where Cox, Rs, ω , and L are the oxide capacitance, source resistance, operating frequency, and length of the transistor, respectively. The size of the cascading transistor M_2 is chosen to be similar that of M_1. This needs a trade-off in order to suppress the noise magnitude of M_2 and the Miller effect of M1.

2.Transistor M_3 is used as LNA biasing network, which forms a current mirror along with M_1. In order to minimize the noise and power consumption, its width must be set to a small fraction of M1's. A good assumption is $W_1 = 20W_3$. Vgs is the gate–source voltage of M_1 and V_{th} is the threshold voltage of the transistors. When the transistors M_1 and M_2 are biased in saturation region and kept far from the triode region, Linearity of LNA is proportional to (Vgs-Vth).The source inductor is used for impedance matching and the gate inductor sets the input resonance frequency. A suitable resistance (Rb) is used to mitigate the effect of gate–source capacitance in transistor M_3 and, its value is arbitrarily chosen to be 2–4 kΩ in 0.18 μm technology. Generally, C_1 is assumed to be 5–10 times larger than C_{gst}. At the output, an inductor is placed at the drain primarily for two reasons. First, the drain inductor should resonate with the total drain capacitance in order to achieve the desired frequency. Second, it should provide a high enough impedance to obtain a good gain.

3.2 The Schematic Diagram and Simulation Results of Integrated CMOS LNA

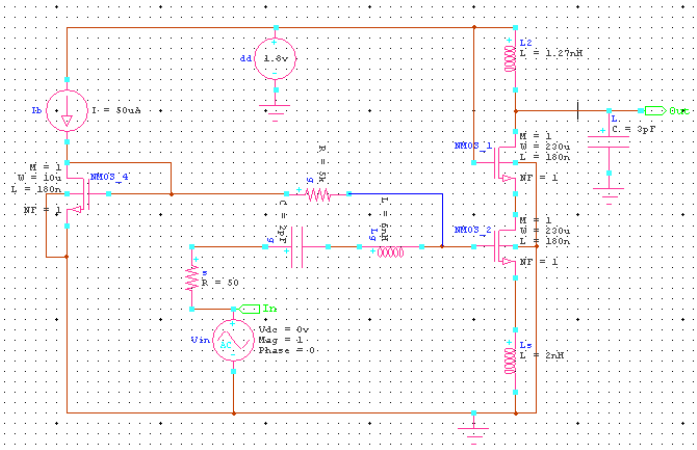

Figure 3.2: The Schematic Diagram of CMOS Integrated LNA.

A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier

This architecture describes a CMOS LNA for Bluetooth/IEEE802.11b front-end receiver in a TSMC 0.18-μm process. The LNA provides a 50Ω input impedance and utilizes a tuned load to provide high selectivity. The LNA achieves a maximum small signal gain of 18.9 dB. The LNA acquires an NF of 2 dB. Differential CMOS LNA have two inputs and two outputs. It has very low noise due to noise rejection nature.

3.2.1 Circuit Implementation:- The proposed differential cascade LNA is shown in Fig.4.6. The inductively degenerated CS input consists of transistors M1-M2, and gate and source inductors, Ls and Lg, respectively. The use of inductive source degeneration through Ls has the benefit of simultaneous input and noise matching. At the input, the off-chip capacitor C_5 is a DC blocking capacitor. For input matching purpose we also used

an off chip capacitor C_7 (~500 fF). A small value of shunt capacitance C_9 (~ 110 fF) at the input optimizes the gain and noise of the LNA. Transistors M5 and M6, known as cascade devices, form a common gate stage, cascade the input stage. The advantage of using the cascade device is that, it basically shields the output from the input stage. It highly increases the reverse isolation. The common gate stage presents low input impedance leading to a low voltage gain in the input stage. In order to improve both the linearity and gain, we used a constant CMOS gm cell. The devices M3 and M4 places together with input transistors in parallel form which use as a gm cell. The aspect ratios of the matching transistors M3 and M4 (10- µm/1.8-µm) are different than the matching transistors M1 and M2 (80-µm/1.8-µm). In this configuration, each input differential pair behaves a reasonably linear transconductance over a small specified input voltage range. Thus, the overall transconductance is the sum of the individual offset transconductance and can be made roughly constant over an almost arbitrary large range of input voltage. At the output, the inductors L_{15} and the capacitors C_1, C_2 and the total drain-node capacitance of M3 and M4 compose an output LC resonance tank circuit. The DC current through the cascade stage is determined by the gate voltage of M1 and M2. This is generated by a CMOS gm bias circuit and injected by a high value register to the gate terminal. The robustness in the performance of the LNA depends primarily on the transconductance of the transistors M1- M4. Better circuit performance can be obtained using a constant gm bias circuit. The biasing circuit stabilizes the LNA amplification.

3.2.2 The Schematic Diagram of Differential CMOS LNA:

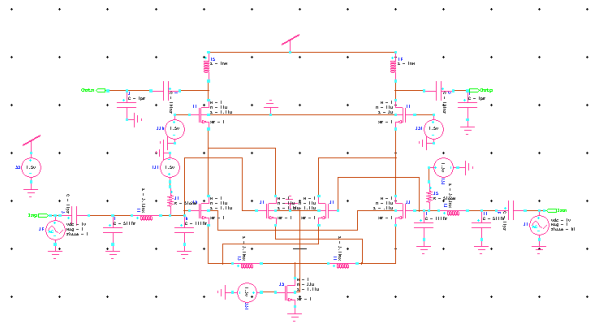

Figure: 4.6 Differential cascode Low Noise Amplifier.

IV. SIMULATION AND RESULTS

FIGURE 4.1: Comparison chart for power Dissipation of fully integrated LNA

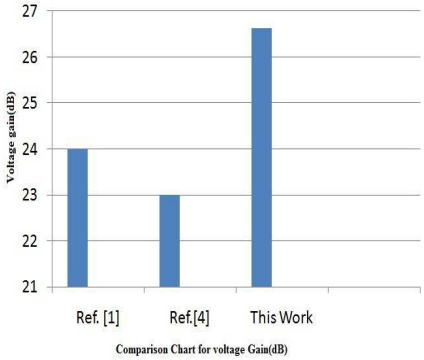

FIGURE 4.2: Comparison chart for Voltage Gain of fully integrated LNA

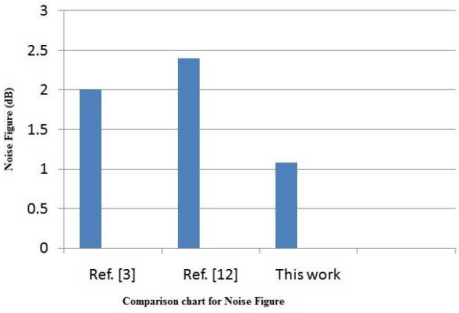

FIGURE 4.3: Comparison of Noise Figure of Differential CMOS LNA

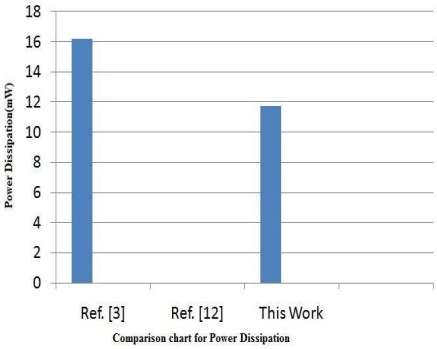

FIGURE 4.4: Comparison of Power Dissipation of Differential CMOS

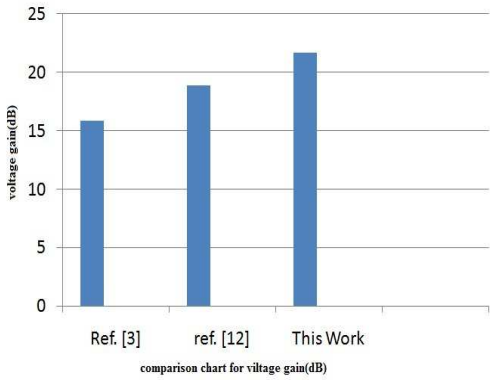

FIGURE 4.5: Comparison of Voltage gain of Differential CMOS LNA

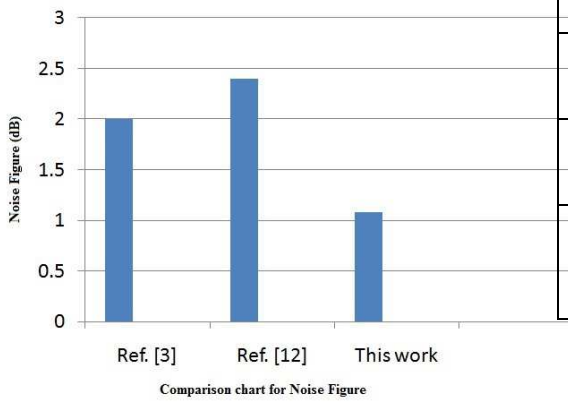

FIGURE 4.6: Comparison of Noise Figure of Differential CMOS LNA

Table 1: Comparison of various parameters of fully integrated LNA

Param-eter	NF (dB)	Voltage Gain (dB)	Phase margin (Degree)	Power Dissipation (mW)	Noise spectral density Input noise (dB)	Output Noise (dB)	Actrans fer function	Technology used	Centre Frequency & BW
Ref.[1]	2	24	-	14.5	-	-	-	0.13	2.45 Ghz
Ref.[2]	7.5	7.1	-	-	-	-	-	90nm	60Ghz
Ref.[2]	7.5	5.6	-	-	-	-	-	90nm	60Ghz
Ref.[3]	2.4	15.87	-	16.2	-	-	-	0.18µm	2Ghz
Ref.[8]	1.910		-	-	-	-	-	0.18µm	2.4Ghz
Ref.[12]	2	18.9	-	-	-	-	-	0.18µm	2.4Ghz
This work	1.08	21.67	67.23^0	11.74	-162.51	-150.22	4.77	0.18µm	2.4Ghz
Ref.[4]	2.6-3	21-25	-	14.5	-	-	-	.13µm	1-5Ghz
Ref.[11]	3.1		-	3mW	-	-	-		5.5Ghz
This work	1.18	26.62	68.19^0	2.65	-179.04	-152.31	21.59	0.18µm	2.4Ghz

Table 4.2: Comparison of various parameters of Differential CMOS LNA

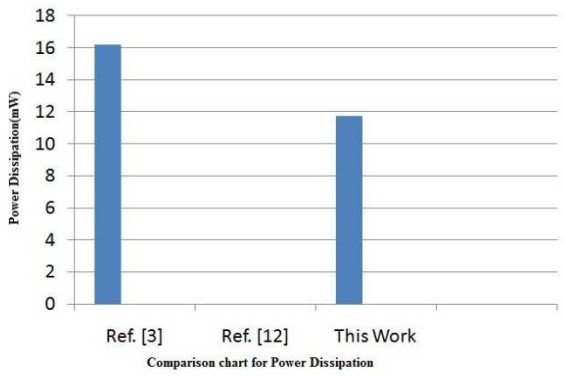

FIGURE 4.7: Comparison of Power Dissipation of Differential CMOS LNA

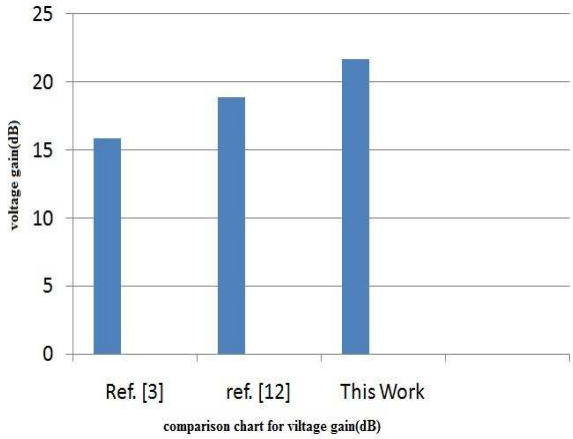

FIGURE 4.8: : Comparison of Voltage gain of Differential CMOS LNA

V. CONCLUSION & FUTURE WORK

5.1 Conclusions

In this thesis work, I designed and simulated two LNA design such as a fully integrated CMOS LNA Differential CMOS LNA with 0.18µm CMOS Technology. Simulation results showed increased voltage gain with lower power consumption. Designed LNA has also better input impedance matching and suitable voltage gain. Hence Different topologies of the Low Noise Amplifier are studied keeping in view the low noise requirements. The inductive source degeneration topology is chosen such that there is no noise due to the input circuitry. With this topology, the required input impedance of around 50Ω is achieved. The output load is a tuned circuit, which is used for output tmpedance matching. The amplifier is first designed to achieve noise optimization. The topology choose produced acceptable results.

5.2 Future Scope

There are many configuration of GaAs LNA and limited configuration of CMOS LNA. So, we can extend our work to design better performance LNA using different strategies. With the advancing technology, inductors of different values, with reasonably good Q values can be integrated for RF circuits. The performance of the circuit can be improved with the availability of a variety of inductor values at hand. The NF and power consumption of the circuit can be still improved from what is achieved in this work.

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